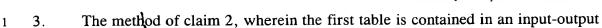
We claim:

1	1/	A method, comprising.
2		providing a first address containing a first number of bits and having an upper
3		portion and a lower portion;
4		comparing the upper portion with a plurality of first entries in a first table;
5		if the upper portion matches a particular one of the plurality of first entries:
6		selecting a second entry in the first table associated with the particular
7		one of the plurality of first entries;
8		combining the second entry with the lower portion to form a first
9		translated address; and
10		transmitting the first translated address.
1	2.—	The method of claim 1 further comprising:
2		if the upper portion does not match any of the plurality of first entries in the
3		first table:
4		accessing a second table having a plurality of third entries;
5		indexing the second table with the upper portion to identify a particular
6		one of the plurality of third entries;
7		combining the particular one of the plurality of third entries with the
8		lower portion to form a second translated address; and
9		transmitting the second translated address.



- 2 controller and the second table is contained in main memory.
- 1 4. The method of claim 2, wherein transmitting the first and second translated
- 2 addresses includes transmitting to a memory controller.
- The method of claim 1, wherein the first table is a translation lookaside
- 2 buffer.
- 1 6. The method of claim 1, wherein providing a first address includes providing a
- 2 first address from a bus controller.
- The method of claim 6, wherein the first table is also used to translate
- addresses-from-a-graphics-controller-

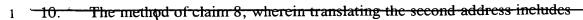
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A method, comprising:

using a conversion table to translate a first address from a graphics controller

- to a memory; and
- using the conversion table to translate a second address from a bus controller
- 5 to the memory.
- 1 9. The method of claim 8, wherein using the conversion table includes using a
- 2 translation lookaside buffer

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- 2 translating the second address to a third address having a different number of bits than
- 3 the second address.
- 1 11. The method of claim 10, wherein translating the first address includes
- 2 translating the first address to a fourth address having a same number of bits as the
- -3 first-address.

12. The method of claim 8, wherein using the conversion table to translate the second address includes:

comparing a first portion of the second address with entries in a first table;

if the first portion matches a particular one of the entries in the first table,

combining a value associated with the particular one with a second

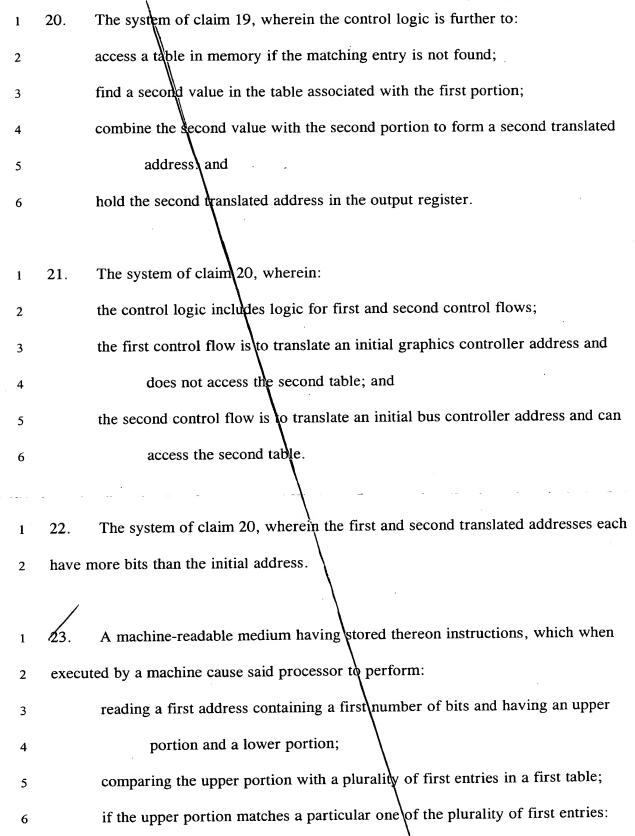
portion of the second address to form a translated address.

- 1 13. The method of claim 12, further comprising:
- 2 if the first portion does not match any of the entries in the first table,
- referring to a second table to translate the second address.
- 1 14. The method of claim 13, wherein:
- 2 comparing includes comparing the first portion of the second address with
- entries in a first table in an input-output controller; and
- referring to the second table includes referring to the second table in main
- 5 memory.

1	15/	An apparatus, comprising:
2		a translation lookaside buffer coupled to an input register and an output
3		register;
4		control logic doupled to the translation lookaside buffer, the input register, and
5		the output register;
6		wherein the control logic is to compare a first portion of an initial address in
7		the input register with entries in the translation lookaside buffer; and if
8		a matching entry is found, to combine a first value associated with the
9		matching entry with a second portion of the initial address to form a
10	٠	first translated address and hold the first translated address in the
11		output register.
1	16.	The apparatus of claim 15, wherein the control logic is further to:
2		access a table in memory if the matching entry is not found;
3		find a second value in the table associated with the first portion;
4		combine the second value with the second portion to form a second translated
5		address: and
6		hold the second translated address in the output register.
1	17.	The apparatus of claim 16, wherein:
2		the control logic includes logic for first and second control flows;
3		the first control flow is to translate an initial graphics controller address and
4		does not access the second table; and

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5	the second control flow is to translate an initial bus controller address and can
6	access the second table.
1	18. The apparatus of claim 16, wherein the first and second translated addresses
2	each have more bits than the initial address.
1	19. A system, including:
2	a processor;
3	a memory;
4	a graphics controller;
5	a bus controller;
6	an input-output controller coupled to the processor, memory, graphics
7	controller and bus controller, the input-output controller including:
8	a translation lookaside buffer coupled to an input register and an output
9	register;
10	control logic coupled to the translation lookaside buffer, the input
11	register, and the output register;
12	wherein the control logic is to compare a first portion of an initial
13	address in the input register with entries in the translation
14	lookaside buffer; and if a matching entry is found, to combine a
15	first value associated with the matching entry with a second
16	portion of the initial address to form a first translated address
17	and hold the first translated address in the output register.



7		selecting a second entry in the first table associated with the particular
8		dne of the plurality of first entries;
9		combining the second entry with the lower portion to form a first
10		translated address; and
		transmitting the first translated address.
11		transmitting the first translated address.
1	24.	The medium of claim 23, further comprising:
2		if the upper portion does not match any of the plurality of first entries in the
3		first table:
4		accessing a second table having a plurality of third entries;
5		indexing the second table with the upper portion to identify a particular
6		one of the plurality of third entries;
7		combining the particular one of the plurality of third entries with the
8	-	lower portion to form a second translated address; and
9		transmitting the second translated address.
,1	25.	The medium of claim 24, wherein the first table is contained in an input-
2	output	controller and the second table is contained in main memory.
1	26.	The medium of claim 24, wherein transmitting the first and second translated
2	addres	sses includes transmitting to a memory controller.
1	27.	The medium of claim 23, wherein the first table is a translation lookaside
2	buffer	<u> </u>

- 1 28. The medium of claim 23, wherein providing a first address includes providing
- 2 a first address from a bus controller.
- 1 29. The medium of claim 28, wherein the first table is also used to translate
- 2 addresses-from a graphics controller.

